Overview

Tezzaron Semiconductor announces a new electronic memory technology – 3T-iRAM – designed to out-perform the fastest memory devices currently on the market. The unique, patented design of 3T-iRAM is a proven and producible technology. The original design was invented in 1998 and produced on successful custom chips; now this mature technology is ready to implement in commercial memory devices.

Electronic memory comes in many varieties to suit the various needs of the industry. The most popular variety is DRAM, a compact and economical technology that is hampered by its slow speed. When it comes to speed, the standout memory technology is SRAM – it is simply the fastest electronic memory available. SRAM is more expensive than DRAM, less reliable, and takes up more space, but its speed advantage is undeniable.

Tezzaron's new 3T-iRAM technology will challenge SRAM by offering better speed, better reliability, smaller size, lower power requirements, and a larger profit margin. 3T-iRAM will also appeal to a large segment of the DRAM market by providing a tremendous speed advantage without sacrificing reliability or density. The result will be a clear market winner, certain to capture a large share of the SRAM market and the high end of the DRAM market, providing a sizeable return to its investors.

The Memory Market

DRAM

The lion's share of the electronic memory market belongs to DRAM, with predicted revenues of US$26.65 Billion in 2004[1]. No other technology can touch DRAM for huge memory capacity at low cost. The biggest challenge to DRAM is the increasing demand for faster memory. In many applications, memory speed is a critical bottleneck; for example, modern microprocessors are forced to sit idle for up to 100 clock cycles each time they wait for their main memory to respond.[2] Many DRAM customers are eager for more speed, but will not switch to SRAM because of size and reliability issues. Tezzaron's fast 3T-iRAM devices will target these customers with high capacity and DRAM-level reliability.

SRAM

In 2004, SRAM market revenues are expected to be about US$3.87 Billion.[1] The SRAM market consists of customers who value memory speed above all else. DRAMs are smaller, more reliable, and much more economical, but when there is an overriding need for speed, customers buy SRAM. Tezzaron will directly target these customers with the superior performance of 3T-iRAM.

1T SRAM Replacement

Another technology that that targets the SRAM market is called "1T replacement". Memory devices built with 1T are nearly as fast as SRAM, but they cannot compete with 3T-iRAM's clear advantages.* The following discussion compares these technologies.

3T-iRAM Advantages

Speed

One measure of memory speed is access time. For DRAM, the best access time is about 20 nanoseconds. In comparison, today's fastest commercial SRAM can achieve an access time of 4 nanoseconds. The fastest 1T replacements can nearly match this speed, but 3T-iRAM is nearly twice as fast: its access time is a blazing 2.25 nanoseconds! This extra speed provides an immediate, marketable advantage in applications that compete on performance (networking, graphics, etc.).

Reliability

DRAM is a fairly robust memory technology. SRAM memory devices are more sensitive to random data upsets; 1T replacements are sensitive to electrical noise and bit cell leakage. Any of these can cause data corruption in a memory device. The underlying technology of 3T-iRAM is significantly different, and is much less susceptible to data corruption – much like DRAM. This is of special importance to critical and/or remote applications (military, medical, aerospace, etc.).

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* For a technical discussion of 3T-iRAM vs. 1T SRAM Replacement, see page 3 of this document

Size

DRAM cells are the smallest of all; SRAM cells are much larger; 3T-iRAM and 1T replacement cells are between the two extremes. Smaller cells can be packed more densely and can store more data in the same space – a big plus. Saving space is crucial in miniaturized applications (embedded devices, spacecraft).

Power

Any memory technology can be built to different specifications, improving one measurement by sacrificing another: building larger cells can increase cell speed, reducing speed can reduce power requirements, and so on. However, when all else is equal, 3T-iRAM runs on a much lower power budget than DRAM, SRAM, or 1T replacement. Low power translates to less heat and longer battery life, two valuable assets.

Cost

3T-iRAM uses about half as much silicon as SRAM does, and has a 10% lower processing cost than 1T. Even at SRAM price parity, 3T-iRAM will turn a tidy profit. 3T-iRAM will not challenge DRAM on cost; however, the superior performance of Tezzaron's devices should easily outweigh the price difference in the high-end market.

Product Status and Plans

August, 2003: Prototypes Announced

Successful prototypes, built in a 90-nm process, demonstrated extraordinary speed and captured world-wide attention.[3]

February, 2004: High-Density Design in Fabrication

These advanced prototypes incorporate unique multi-bit cells, storing four times as much data per cell as the first prototypes. Finished devices are expected in June of 2004.

Q4 of 2004: 72Mb Drop-In SRAM Replacements

These devices will exactly replicate the size and behavior of today's largest fast SRAMs. This point-for-point equivalence will allow customers to implement the new technology without altering their products or designs. Although these devices will not exhibit speed or size advantages, they will provide higher reliability and draw less power than the SRAMs they replace.

Q1 of 2005: 72Mb High-Speed

The true speed of 3T-iRAM will shine through in these devices. The success of the drop-in parts will have established our technology, so customers will be willing to modify their designs to take advantage of the great speed offered by these non-standard parts.

Future Parts

144Mb Stacked

Tezzaron's FaStack™ process will integrate two layers of high-speed 3T-iRAM for twice the capacity in the same footprint. T\he large capacity and excellent reliability of this product will appeal to the high end of the DRAM market as well as the traditional SRAM market.

144Mb Non-Stacked (Monolithic)

Advanced processing will build twice the capacity in a single layer, providing even more speed than previous versions at a lower production cost.

288Mb Stacked

Integrating two layers of the new, smaller cells will double the capacity yet again, producing the fastest, densest memory devices in the SRAM market, with strong appeal to the huge DRAM market as well.

Conclusion

Tezzaron's 3T-iRAM will outperform today's fastest memory devices and bridge the gap between the SRAM and DRAM markets. The potential for revenue and growth is extraordinary. Tezzaron is very interested in acquiring industry partners and private investment to further exploit this ground-breaking technology.

Appendices

Glossary and Pronunciation

3T-iRAM™ (three-tee-EYE-ram) – Tezzaron's trademark name for a three-transistor current-sensing RAM technology. 3T signifies the three-transistor design, and "i" is the engineering symbol for electrical current.

DRAM (DEE-ram) – Dynamic RAM – Today's densest, most economical memory technology.

FaStack™ (FAST-ack) – Tezzaron's unique wafer stacking technology for building 3D integrated circuits.

Mb – Megabit – 1,048,576 bits

Monolithic (monn-oh-LITH-ick) – in one piece; not stacked.

PSiRAM™ (SIGH-ram) – an earlier name for 3T-iRAM

RAM (ram) – Random Access Memory – Electronic memory that can be accessed in any sequence and can be changed (re-written) at will.

SRAM (ESS-ram) – Static RAM – Today's fastest memory technology.

Technical Discussion

Design

Tezzaron's SRAM replacement technology, 3T-iRAM, is based on an innovative three-transistor DRAM-type cell. The design isolates the data storage capacitor from the bitline, providing amplification, local ground referencing, and nondestructive reads. Tezzaron has produced a handful of different implementations that allow multiport creation, or overlapping of read and write operations, or hidden refresh.

As SRAM continues to shrink, leakage and upset issues become more and more difficult to solve. The most obvious solution is to move to a dynamic memory structure. DRAM structures in general have less leakage and less sensitivity to ionization energy than SRAM, and dynamic memory implementations for SRAM replacement are generally half the size of static memory in the same process. A popular alternative today is 1T SRAM replacement, which acts and looks very much like DRAM, with appropriate mechanisms to hide refresh. The Tezzaron 3T-iRAM approach has all the significant benefits of typical 1T implementations with added advantages in scaling, noise tolerance, leakage, and performance.

For reference, this discussion compares 3T-iRAM to the MoSys 1T SRAM replacement technology, but the comparison is generally applicable to all 1T memories.

Speed

3T-iRAM achieves its unprecedented speed by sensing *current* rather than *voltage*. In memory circuits, the current changes faster than the voltage does, so a change in current can be detected and reported more quickly than a change in voltage. 3T-iRAM exploits this difference without radically changing the standard DRAM design, thus achieving SRAM-like speeds with DRAM-like reliability.

Scaling

The continued scaling of semiconductors presents significant challenges to SRAM replacements: as geometry scales down, bit cell capacitance shrinks and parasitic capacitance increases. At 90nm, the bit cell capacitance is 1-2ff for MoSys as well as Tezzaron, with bitline capacitance of ~.33ff/µm.

In 1T SRAM replacements, the bit cell state is sensed by deflection of the bitline – for adequate signal margin, 50mV of signal deflection is required. Given a 1V stored charge, the maximum bit cell to bitline ratio is ~20, or about 64 bits/bitline. This assumes no leakage and a reasonable noise floor. Further, this limitation is independent of access time (speed). It is safe to assume that at 65nm the 1T issues will force the bitlines to be half of their current size or even less. This implies that 1T array efficiency will be cut in half and that effective bit size will significantly increase.

In contrast to 1T implementations, 3T-iRAM cell operation is independent of bitline capacitance because the storage capacitor is isolated from the bitline during reads. The only bitline limitation is leakage, which does not become an issue until bits/bitline is >>1024; therefore, array efficiency is maintained as scaling continues.

Noise

Noise is a major concern in 1T SRAM replacements. Coupled noise sensitivity demands extra care to isolate power, provide shielding, and control substrate noise. This results in stringent layout dependencies and "no route over" restrictions. Frequently, 1T SRAM designs require a shield layer.

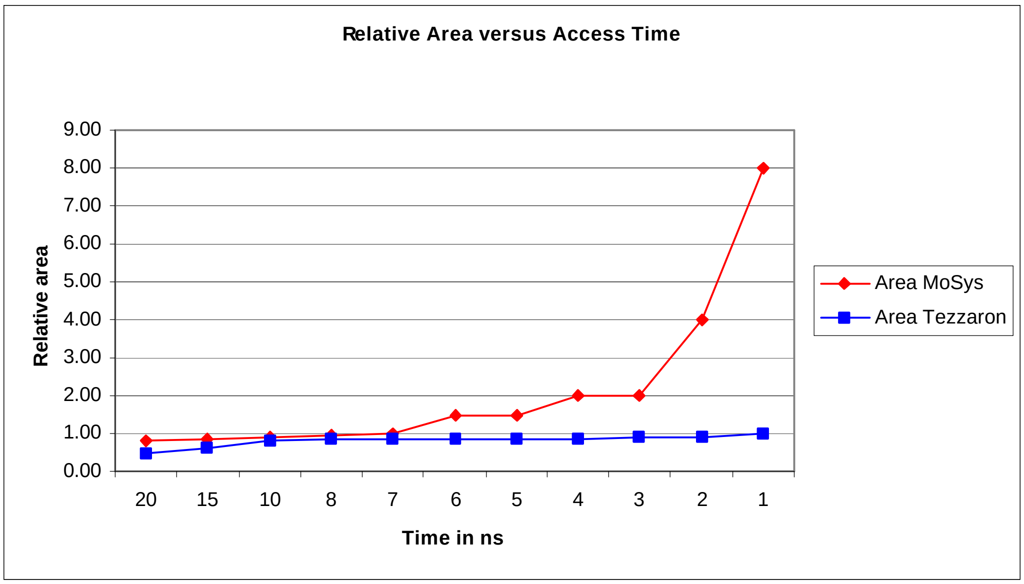
Using 3T-iRAM relieves most of these concerns. Because the primary bit sensing takes place in the bit cell itself, with extremely localized sensing, 3T-iRAM memories suffer virtually no noise issues. This results in additional layout freedom and no shield requirements. "Route over" is also generally permitted. The 3T-iRAM signal is rail to rail; therefore, noise tolerance is extremely good. The 3T-iRAM cell can operate with a noise floor of hundreds of millivolts.

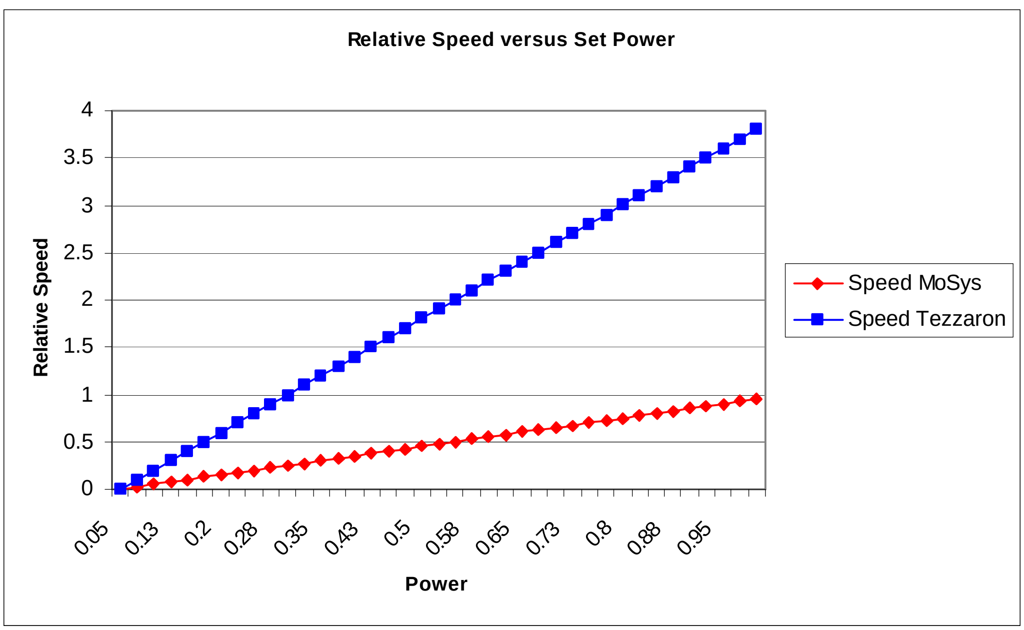
Bit Cell Leakage

Leakage from the bit cell capacitor is a big concern in any dynamic memory device. In 1T cells, drooping bit cell voltage directly compromises the ability to sense the actual data. A 50% drop in pre-refresh voltage dictates a 50% reduction in the number of bits per bitline to maintain the same signal level in a 1V system.

3T-iRAM also is affected by leakage. However, drooping bit cell voltage does not compromise the ability to sense the data until the stored voltage drops below Vt. Data loss does not occur unless pre-refresh voltage drops by 65%-80%, and the bitline length has no effect. Given that leakage is an exponential function, this reduced sensitivity to leakage means that 3T-iRAM refresh can occur 2 to 5 times less often, yielding a 2- to 5-fold reduction in standby power.

Performance Trade-Offs





Other Technical Considerations

The discussions above deal with "logic only" processing, but even in an embedded DRAM process, 3T-iRAM still offers significant benefits over 1T. In particular, 3T-iRAM always out-performs 1T in terms of speed because of the additional in-cell amplifier.

Tezzaron's 3T SRAM replacement technology is silicon proven down to 90nm. It has demonstrated sub-nanosecond access times in memory arrays as large as 32Mb. At 90nm, 3T-iRAM cells are 0.59 square microns per bit with greater than 70% array efficiency; for comparison, the same process yields SRAM at 1.25 square microns per bit. Tezzaron's 3T-iRAM cells are easily ported to other processes, and have already been fabricated in several fabs and various technologies. 3T-iRAM is ideal for SoCs, graphics processors, and main CPU cache opportunities.

References

[1] Gartner Dataquest, April 2004

[2] Amol Baksi and others, "Memory Latency: to Tolerate or to Reduce?" (Los Angeles, California: University of Southern California, Department of Electrical Engineering – Systems), page 1.

[3] Press Release: "New Memory Technology is World's Fastest" 18 August, 2003 http://www.tezzaron.com/about/Press/release180803.htm – Picked up by Silicon Strategies, EE Times, EETimes IP/SoC Newsletter, Design and Reuse, TechNewsWorld, EE Design, CommsDesign, The Work Circuit, Science News; **UK:** EE Times UK; **Taiwan:** EE Times Taiwan; **Finland:** Prosessori; **Belarus:** KB Online, "Zhelezniy"; **China:** CCW, China Semiconductor Industry Association, Electron.Cetin, ETIRI, EE Times China; **Russia:** Compulenta, Computerra, Inforser, Ak-Cent Microsystems, DELFI, Alta Plus, Business Online, Saturn-Plus, Roscomputer, XXP-Design, Crosna Space Communications, Caspian World News, Talk.Mail/Forum, ITInfo, PCSamara, IVEN Computers, RussianPhiladelphia, F-Center, PCHard, HomePC, Ferra, iBusiness, Rostov, CPrice Info, EZPC, TechnoStyle, ProComputer Hotline, GoldSoft, Computer News, ArtCom, XKP; **Ukraine:** Alser MyComp, Gazeta 2000, Corason; **Latvia:** digital times, AK-Cents Microsystems; **Korea:** EE Times Korea, iCON, ECRC, ICAT; **Lithuania:** Takas; **Kazakhstan:** Computers; **Moldova:** NewsGate; **Germany:** FinanzNachrichten; and others. For links to these sites, see http://www.tezzaron.com/about/Press/news.html .