

**72Mb Synchronous Double Transfer Rate (DTRII™) 3T-iRAM™
With Common I/O**

**Burst of 4
SRAM-Compatible**

Features

- Error-resistant 3T-iRAM™ technology
- DTRII™ Interface with Common I/O bus
- Fully pin-compatible with DDRII and SigmaCIO™ SRAMs
- JEDEC-standard pinout and package
- Burst of 4 Read and Write (Byte Writes)
- 1.8 V +100/-100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation with self-timed Late Write
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump 15mm x 17mm BGA, 1 mm bump pitch
- Pin-compatible with 9Mb, 18Mb, 36Mb, and 144Mb devices

Options

- Configurations: 8M x 9 C09
4M x 18 C18
2M x 36 C36
- Package: 165 FBGA B
- Speed (MHz): 333 MHz -333
300 MHz -300
200 MHz -200
167 MHz -167

Marking

Part number example: **TSC3D472C18B-300**

Functional Description

3T-iRAM™ is a unique type of dynamic memory. Tezzaron has crafted these pseudo-static devices to provide entirely SRAM-compatible interfaces and timing. The unique design of these 3T memories provides soft error rates up to 10 times lower than equivalent high-speed, high-density SRAMs.

DTRII™ is a double transfer rate interface that makes these devices drop-in compatible with DDRII and SigmaCIO™ SRAMs.

These synchronous 72Mb 3T-iRAM devices employ two input register clocks, K and \bar{K} . The user can manipulate the output register clocks quasi-independently with C and \bar{C} . These clocks are four independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

These devices always transfer data in four packets, but addressing is handled differently for x9 parts than for x36 and x18 parts:

For x36 and x18, when a new address is loaded, A0 and A1 preset an internal 2 bit address counter. The counter increments by 1 for each beat of a burst of four data transfer, wrapping to 00 after reaching 11.

For x9, when a new address is loaded, the LSBs are internally set to 00 for the first read or write transfer, and incremented by 1 for the next three transfers.

Speed Parameter Synopsis:
(all units ns)

	-333	-300	-250	-200	-167
tKHKH	3.00	3.30	4.00	5.00	6.00
tKHQV	0.45	0.45	0.45	0.45	0.50

2M x 36: Top View

11 x 15 Bump BGA – 15 x 17 mm² Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	NC	SA	R / \overline{W}	$\overline{BW2}$	\overline{K}	$\overline{BW1}$	\overline{LD}	SA	SA	CQ	A
B	NC	DQ27	DQ18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	NC	NC	DQ8	B
C	NC	NC	DQ28	Vss	SA	SA0	SA1	Vss	NC	DQ17	DQ7	C
D	NC	DQ29	DQ19	Vss	Vss	Vss	Vss	Vss	NC	NC	DQ16	D
E	NC	NC	DQ20	VDDQ	Vss	Vss	Vss	VDDQ	NC	DQ15	DQ6	E
F	NC	DQ30	DQ21	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ5	F
G	NC	DQ31	DQ22	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ14	G
H	\overline{Doff}	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	DQ32	VDDQ	VDD	Vss	VDD	VDDQ	NC	DQ13	DQ4	J
K	NC	NC	DQ23	VDDQ	VDD	Vss	VDD	VDDQ	NC	DQ12	DQ3	K
L	NC	DQ33	DQ24	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2	L
M	NC	NC	DQ34	Vss	Vss	Vss	Vss	Vss	NC	DQ11	DQ1	M
N	NC	DQ35	DQ25	Vss	SA	SA	SA	Vss	NC	NC	DQ10	N
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0	P
R	TDO	TCK	SA	SA	SA	\overline{C}	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to DQ0:DQ8;
 $\overline{BW1}$ controls writes to DQ9:DQ17;
 $\overline{BW2}$ controls writes to DQ18:DQ26;
 $\overline{BW3}$ controls writes to DQ27:DQ35.

4M x 18: Top View

11 x 15 Bump BGA – 15 x 17 mm² Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	SA	SA	R / \overline{W}	$\overline{BW1}$	\overline{K}	NC	\overline{LD}	SA	SA	CQ	A
B	NC	DQ9	NC	SA	NC	K	$\overline{BW0}$	SA	NC	NC	DQ8	B
C	NC	NC	NC	Vss	SA	SA0	SA1	Vss	NC	DQ7	NC	C
D	NC	NC	DQ10	Vss	Vss	Vss	Vss	Vss	NC	NC	NC	D
E	NC	NC	DQ11	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ6	E
F	NC	DQ12	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ5	F
G	NC	NC	DQ13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC	G
H	\overline{Doff}	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ	H
J	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	DQ4	NC	J
K	NC	NC	DQ14	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ3	K
L	NC	DQ15	NC	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2	L
M	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	DQ1	NC	M
N	NC	NC	DQ16	Vss	SA	SA	SA	Vss	NC	NC	NC	N
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0	P
R	TDO	TCK	SA	SA	SA	\overline{C}	SA	SA	SA	TMS	TDI	R

Notes: $\overline{BW0}$ controls writes to DQ0:DQ8;
 $\overline{BW1}$ controls writes to DQ9:DQ17

8M x 9: Top View

11 x 15 Bump BGA – 15 x 17 mm² Body – 1 mm Bump Pitch

	1	2	3	4	5	6	7	8	9	10	11	
A	\overline{CQ}	SA	SA	R/ \overline{W}	NC	\overline{K}	NC	\overline{LD}	SA	SA	CQ	A
B	NC	NC	NC	SA	NC	K	\overline{BW}	SA	NC	NC	DQ4	B
C	NC	NC	NC	V _{SS}	SA	NC	SA	V _{SS}	NC	NC	NC	C
D	NC	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	NC	D
E	NC	NC	DQ5	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	DQ3	E
F	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC	F
G	NC	NC	DQ6	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC	G
H	\overline{Doff}	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ	H
J	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ2	NC	J
K	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC	K
L	NC	DQ7	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	DQ1	L
M	NC	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	NC	M
N	NC	NC	NC	V _{SS}	SA	SA	SA	V _{SS}	NC	NC	NC	N
P	NC	NC	DQ8	SA	SA	C	SA	SA	NC	NC	DQ0	P
R	TDO	TCK	SA	SA	SA	\overline{C}	SA	SA	SA	TMS	TDI	R

Notes: Unlike the x36 and x18 versions of this device, the x9 does not give the user access to address bits 0 and 1. The least significant address bits are set to 00 at the beginning of each access.

Pin Descriptions

Symbol	Type	Description
SA	INPUT	Synchronous address inputs
SA0, SA1	INPUT	Least significant address bits For x36 and x18: user input to the burst counter For x9: internally set to 00
NC	---	No connect; not connected to die or any other pin
$\overline{R} / \overline{W}$	INPUT	Synchronous read/write
$\overline{BW0} - \overline{BW3}$	INPUT	Byte write controls
\overline{LD}	INPUT	Synchronous load
K / \overline{K}	INPUT	Input clocks (positive/negative)
C / \overline{C}	INPUT	Output clocks (positive/negative)
TMS	INPUT	Test mode select
TDI	INPUT	Test data input
TCK	INPUT	Test clock
TDO	OUTPUT	Test data output
VREF	INPUT	HSTL input reference voltage
ZQ	INPUT	Output impedance matching input
DQ	I/O	Data; three-state
\overline{Doff}	INPUT	Disable DLL (when low)
$\overline{CQ} / \overline{CQ}$	OUTPUT	Output echo clock (positive/negative)
VDD	SUPPLY	Power supply; 1.8 V nominal
VDDO	SUPPLY	Isolated output buffer supply; 1.5 V nominal
VSS	SUPPLY	Ground

Functional Details

Background

Common I/O SRAMs, from a system architecture point of view, are attractive in read dominated or block transfer applications. Therefore, this device's interface and truth table are optimized for burst reads and writes. Common I/O SRAMs are unpopular in applications where alternating reads and writes are needed because bus turnaround delays can cut high speed Common I/O SRAM data bandwidth in half.

Burst Operations

Read and write operations are "burst" operations. In every case where a read or write command is accepted by the RAM, it responds by issuing or accepting four beats of data, executing a data transfer on subsequent rising clock edges, as illustrated in the timing diagrams. It is not possible to stop a burst once it starts; four beats of data are always transferred. This means that it is possible to load new addresses every other K clock cycle. Addresses can be loaded less often, if intervening deselect cycles are inserted.

Deselect Cycles

Chip Deselect commands are pipelined to the same degree as read commands. This means that if a deselect command is applied to the RAM on the next cycle after a read command, the device will complete the four beat read data transfer and then execute the deselect command, returning the output drivers to high-Z. A high on the \overline{LD} pin prevents any read or write commands and puts the RAM into deselect mode as soon as it completes any outstanding burst transfer operations.

Read Cycles

This device executes pipelined reads. The Address, \overline{LD} , and R/\overline{W} pins are evaluated on a rising edge of K. If \overline{LD} is low and R/\overline{W} high, a read command is clocked into the RAM on that edge. After the next rising edge of K, the RAM produces data out in response to the next rising edge of \overline{C} (or the next rising edge of \overline{K} , if C and \overline{C} are tied high). Three more beats of data are transferred on the next three rising edges of C, \overline{C} , and C for a total of four transfers per address load.

Write Cycles

This device executes "late write" data transfers. The Address, \overline{LD} and R/\overline{W} pins are evaluated on a rising edge of K. If \overline{LD} and R/\overline{W} are low, a write command and its address are clocked into the RAM on that edge. Data in is due at the device inputs on the next rising edge of K. To complete the remaining beats of the burst of four write transfer, the RAM captures data in on the next three rising edges of \overline{K} , K, and \overline{K} for a total of four transfers per address load.

Power-Up Sequence

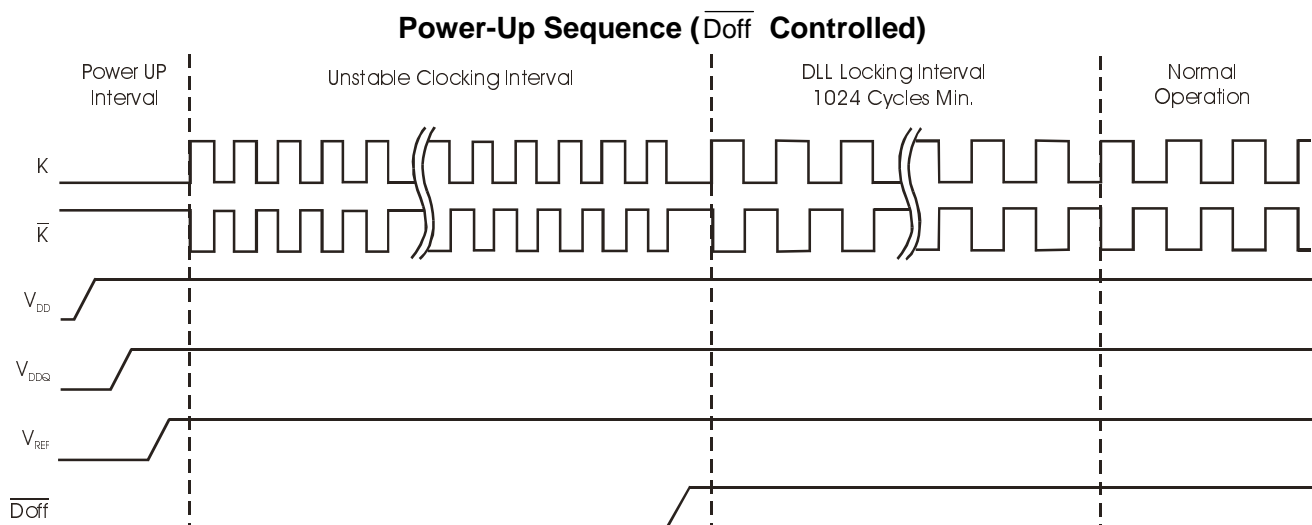
These devices must be powered up in a specific sequence in order to avoid undefined operations.

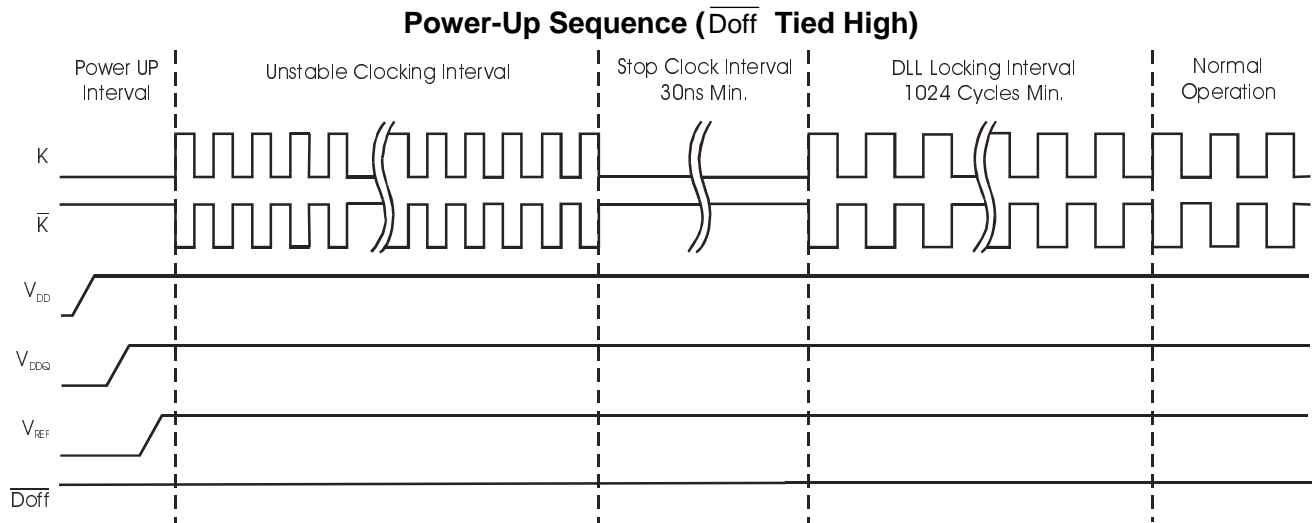
1. Power-up and maintain \overline{Doff} at low state.
 - 1a. Apply VDD.
 - 1b. Apply VDDQ.
 - 1c. Apply VREF (may also be applied at the same time as VDDQ).
2. After power is achieved and clocks (K, \overline{K} , C, \overline{C}) are stabilized, change \overline{Doff} to high.
3. An additional 1024 clock cycles are required to lock the DLL after it has been enabled.

Note: If you want to tie \overline{Doff} high with an unstable clock, you must stop the clock for a minimum of 30 ns to reset the DLL after the clocks become stabilized.

DLL Constraints

- The DLL synchronizes to either K or C clock. These clocks should have low phase jitter (see t_{KCVAR} on page 14).
- The DLL cannot operate at a frequency lower than 119 MHz.
- If the incoming clock is not stabilized when DLL is enabled, the DLL may lock on the wrong frequency and cause undefined errors or failures during the initial stage.
- If the frequency is changed, DLL reset is required. After reset, a minimum of 1024 cycles is required for DLL lock.





Special Functions

Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{\text{BW0}}$ for the D0–D8 inputs) inhibits the storage of that particular byte, leaving whatever data may be stored at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a four beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Example: x18 Write Sequence Using Byte Write Enables

Data In Sample Time	$\overline{\text{BW0}}$	$\overline{\text{BW1}}$	D0–D8	D9–D17
Beat 1	0	1	Data In	X
Beat 2	1	0	X	Data In
Beat 3	0	0	Data In	Data In
Beat 4	1	0	X	Data In

Notes: “1” = input “high”; “0” = input “low”; “X” = input “don’t care”.

Resulting Write Operation

Byte 1 D0–D8	Byte 2 D9–D17	Byte 3 D0–D8	Byte 4 D9–D17	Byte 5 D0–D8	Byte 6 D9–D17	Byte 7 D0–D8	Byte 8 D9–D17
Written	Unchanged	Unchanged	Written	Written	Written	Unchanged	Written
Beat 1		Beat 2		Beat 3		Beat 4	

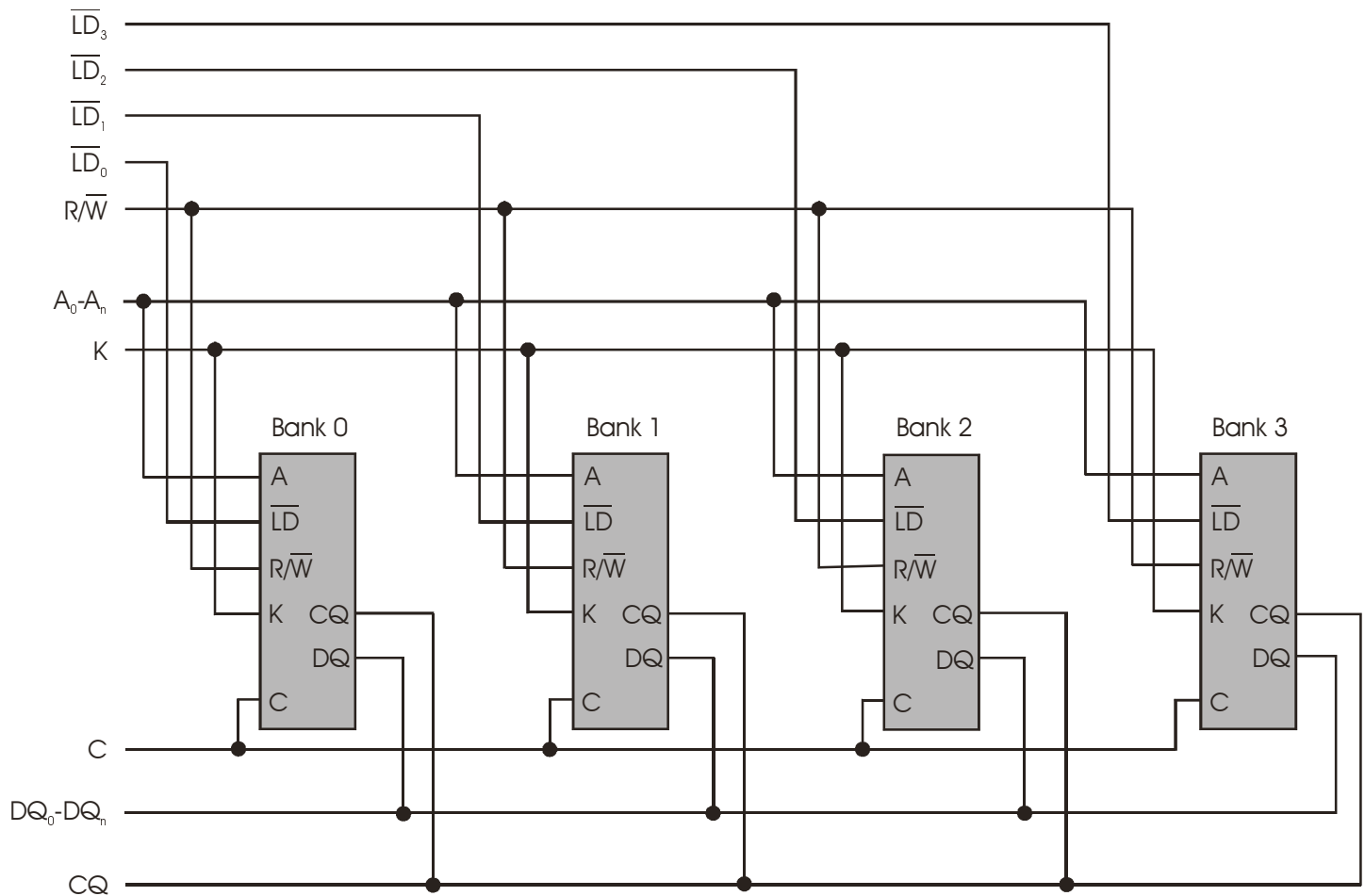
Output Register Control

This memory device offers two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and \bar{C} . These inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and \bar{K} clocks. If the C and \bar{C} clock inputs are tied high, the RAM reverts to K and \bar{K} control of the outputs, allowing the device to function as a conventional pipelined read SRAM.

Depth Expansion

Depth Expansion requires replicating the \bar{LD} signal for each bank, as shown in the following diagram. All other control signals can be common between banks as appropriate.

Example Four Bank Depth Expansion Schematic



Note: For simplicity, this diagram does not show $\bar{B}W_n$, \bar{K} , and \bar{C} .

Output Driver Impedance Control

This memory device is supplied with an optional programmable impedance output driver that can periodically readjust the output driver impedance to compensate for drifts in supply voltage and temperature.

To enable this feature, the ZQ pin must be connected to VSS via an external resistor, RQ, with a value 5X the value of the desired RAM output impedance. The allowable range of RQ is between 175Ω and 350Ω. An internal calibration sequence occurs every 1024 cycles, and an update is performed during the next available deselected memory cycle. Each update may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

To disable this feature, the ZQ pin may be tied directly to VDDQ. The device then runs with a constant minimum impedance; no calibration or adjustments are performed.

Common I/O Truth Table

Function	K_n	\overline{LD}	R / \overline{W}	DQ A+ 0	DQ A + 1
Deselect	•	1	X	Hi-Z	Hi-Z
Write	•	0	0	$D@K_{n+1}$	$D@K_{n+1}$
Read	•	0	1	$Q@K_{n+1}$ or \overline{C}_{n+1}	$Q@K_{n+2}$ or C_{n+2}

Notes: X = Don't Care; Q is controlled by K clocks if C clocks are not used.

Byte Write Clock Truth Table

Function	\overline{BW} K↑ (t_{n+1})	\overline{BW} K↑ ($t_{n+1/2}$)	\overline{BW} K↑ (t_{n+2})	\overline{BW} K↑ ($t_{n+2 1/2}$)	D K↑ (t_{n+1})	D K↑ ($t_{n+1/2}$)	D K↑ (t_{n+2})	D K↑ ($t_{n+2 1/2}$)
Write: Dx stored if $\overline{BW}_n = 0$ in all four data transfers	T	T	T	T	D1	D2	D3	D4
Write: Dx stored if $\overline{BW}_n = 0$ in first data transfer only	T	F	F	F	D1	X	X	X
Write: Dx stored if $\overline{BW}_n = 0$ in second data transfer only	F	T	F	F	X	D2	X	X
Write: Dx stored if $\overline{BW}_n = 0$ in third data transfer only	F	F	T	F	X	X	D3	X
Write: Dx stored if $\overline{BW}_n = 0$ in fourth data transfer only	F	F	F	T	X	X	X	D4
Write Abort: No Dx stored in any data transfer	F	F	F	F	X	X	X	X

Notes: "1" = input "high"; "0" = input "low"; "X" = input "don't care";
 "T" = input "true"; "F" = input "false".
 If one or more $\overline{BW}_n = 0$, then $\overline{BW} = "T"$, else $\overline{BW} = "F"$.

x36 Byte Write Enable Truth Table

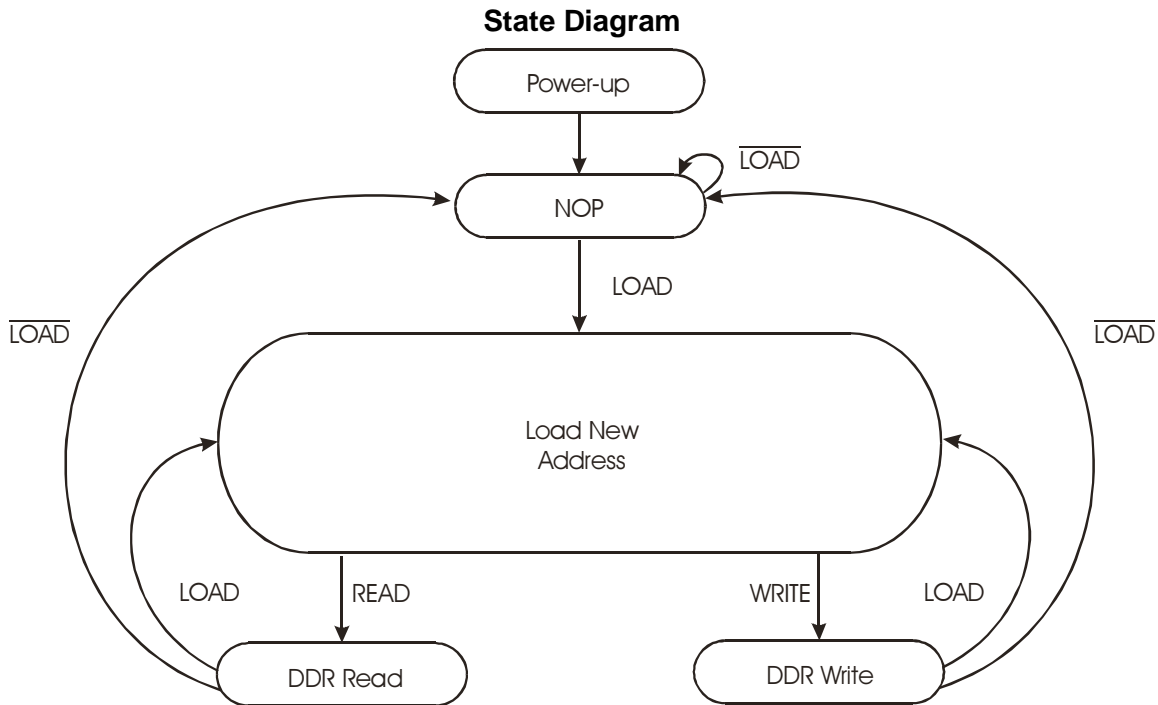
$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0 – D8	D9 – D17	D18 – D26	D27 – D35
1	1	1	1	X	X	X	X
0	1	1	1	Data	X	X	X
1	0	1	1	X	Data	X	X
0	0	1	1	Data	Data	X	X
1	1	0	1	X	X	Data	X
0	1	0	1	Data	X	Data	X
1	0	0	1	X	Data	Data	X
0	0	0	1	Data	Data	Data	X
1	1	1	0	X	X	X	Data
0	1	1	0	Data	X	X	Data
1	0	1	0	X	Data	X	Data
0	0	1	0	Data	Data	X	Data
1	1	0	0	X	X	Data	Data
0	1	0	0	Data	X	Data	Data
1	0	0	0	X	Data	Data	Data
0	0	0	0	Data	Data	Data	Data

Notes: “1” = input “high”; “0” = input “low”; “Data” = input data to be written; “X” = input “don’t care”.

x18 Byte Write Enable Truth Table

$\overline{BW0}$	$\overline{BW1}$	D0 – D8	D9 – D17
1	1	X	X
0	1	Data	X
1	0	X	Data
0	0	Data	Data

Notes: “1” = input “high”; “0” = input “low”; “Data” = input data to be written; “X” = input “don’t care”.



Notes: Uses an internal 1-bit address burst counter – i.e., when first address is A0, next internal burst address is A0+1.
 “READ” = read active status with R/W High;
 “WRITE” = write inactive status with R/W Low;
 “LOAD” = read new address active status with \overline{LD} Low;
 “ \overline{LOAD} ” = read new address inactive status with \overline{LD} High.

Absolute Maximum Ratings

(All voltages reference to Vss)

Symbol	Description	Value	Unit
VDD	Voltage: VDD pins	-0.5 to 2.9	V
VDDQ	Voltage: VDDQ pins	-0.5 to VDD	V
VREF	Voltage: VREF pins	-0.5 to VDDQ	V
VI/O	Voltage: I/O pins	-0.5 to VDDQ +0.5 (• 2.9 max.)	V
VIN	Voltage: other input pins	-0.5 to VDDQ +0.5 (• 2.9 max.)	V
IIN	Input current on any pin	+/- 100	mA dc
IOUT	Output current on any I/O pin	+/- 100	mA dc
TJ	Maximum junction temperature	125	°C
TSTG	Storage temperature	-55 to 125	°C

Note: Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Extended exposure to conditions exceeding the Recommended Operating Conditions may affect reliability of this component.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{DD}	1.70	1.8	1.90	V
I/O Supply Voltage	V _{DDQ}	1.40	1.5	V _{DD}	V
Reference Voltage	V _{REF}	0.68	--	0.95	V
Ambient Temperature (Commercial)	T _A	0	25	70	°C
Ambient Temperature (Industrial)	T _A	-40	25	85	°C

Notes: Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both $1.4\text{ V} \leq V_{DDQ} \leq 1.6\text{ V}$ (i.e., 1.5 V I/O) and $1.7\text{ V} \leq V_{DDQ} \leq 1.95\text{ V}$ (i.e., 1.8 V I/O) and quoted at the worst case condition.

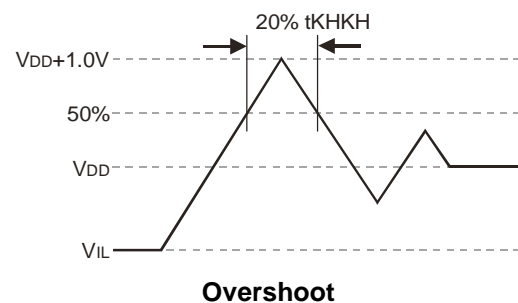
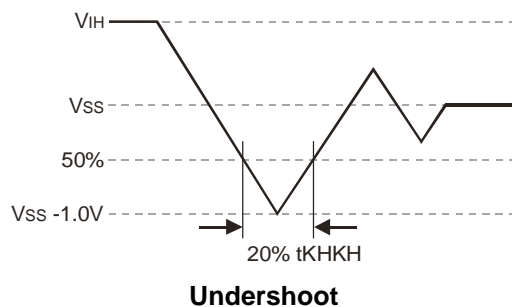
Power supplies must be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}.

HSTL I/O Input Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
DC Input Logic High	V _{IH(DC)}	V _{REF} + 0.10	V _{DDQ} + 0.3	V	1, 2, 3, 4
DC Input Logic Low	V _{IL(DC)}	-0.3	V _{REF} - 0.10	V	1, 2, 3, 4
AC Input Logic High	V _{IH(AC)}	V _{REF} + 0.20	--	V	1, 6, 7
AC Input Logic Low	V _{IL(AC)}	--	V _{REF} - 0.20	V	1, 6, 7
V _{REF} Peak to Peak AC Voltage	V _{REF(AC)}	--	5% V _{REF(DC)}	V	5

- Compatible with both 1.8 V and 1.5 V I/O drivers.
- These are DC test criteria; the DC design criterion is V_{REF} ± 50 mV. V_{IH(AC)} and V_{IL(AC)} levels are defined separately to for measuring timing parameters.
- V_{IL(DC)} Min = -0.3 V, V_{IL(AC)} Min = -1.5 V (pulse width ≤ 3ns).
- V_{IH(DC)} Max = V_{DDQ} + 0.3 V, V_{IH(AC)} Max = V_{DDQ} + 0.85 V (pulse width ≤ 3ns).
- The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
- To guarantee AC characteristics, V_{IL}, V_{IH}, Trise, and Tfall of inputs and clocks must be within 10% of each other.
- For devices supplied with HSTL I/O input buffers.

Undershoot/Overshoot Measurement and Timing



Capacitance (pF)

(TA = 25 °C, f = 1 MHz, VDD = 1.8 V, VDDQ = 1.5 V)

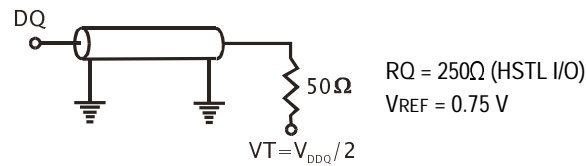
Parameter (sample tested)	Symbol	Test conditions	Typ.	Max.
Input Capacitance	C _{IN}	V _{IN} = 0 V	4	5
Output Capacitance	C _{OUT}	V _{OUT} = 0 V	6	7
Clock Capacitance	C _{CLK}	--	5	6

AC Test Conditions

Parameter	Conditions
Input high level	VDDQ
Input low level	0 V
Maximum input slew rate	2 V/ns
Input reference level	VDDQ/2
Output reference level	VDDQ/2

Note: Test conditions specified with output loading as shown below unless otherwise noted.

AC Test Load Diagram



Input and Output Leakage Characteristics (μA)

Parameter	Symbol	Test Conditions	Min	Max
Input leakage current (except mode pins)	I _{IL}	V _{IN} = 0 to VDDQ	-2	2
Output leakage current	I _{OL}	Output disable, V _{OUT} = 0 to VDDQ	-2	2

AC Electrical Characteristics (ns)

Parameter	Symbol	-333		-300		-250		-200		-167		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock												
K, \overline{K} Clock Cycle Time	tKHKH	3.0	3.5	3.3	4.2	4.0	6.3	5.0	7.88	6.0	8.4	
C, \overline{C} Clock Cycle Time	tCHCH											
tKC Variance (Clock phase jitter)	tKCVar	--	0.2	--	0.2	--	0.2	--	0.2	--	0.2	5
K, \overline{K} Clock High Pulse Width	tKHKL	1.2	--	1.32	--	1.6	--	2.0	--	2.4	--	
C, \overline{C} Clock High Pulse Width	tCHCL											
K, \overline{K} Clock Low Pulse Width	tCLKH	1.2	--	1.32	--	1.6	--	2.0	--	2.4	--	
C, \overline{C} Clock Low Pulse Width	tCLCH											
K to \overline{K} High	tKH \overline{K} H	1.35	--	1.49	--	1.8	--	2.2	--	2.7	--	
C to \overline{C} High	tCH \overline{C} H											
K, \overline{K} Clock High to C, \overline{C} Clock High	tKHCH	0	1.3	0	1.45	0	1.8	0	2.3	0	2.8	
K Static to DLL reset	tKCRreset	30	--	30	--	30	--	30	--	30	--	
Output Times												
K, \overline{K} Clock High to Data Output Valid	tKHQV	--	0.45	--	0.45	--	0.45	--	0.45	--	0.5	3
C, \overline{C} Clock High to Data Output Valid	tCHQV											
K, \overline{K} Clock High to Data Output Hold	tKHQX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.5	--	3
C, \overline{C} Clock High to Data Output Hold	tCHQX											
K, \overline{K} Clock High to Echo Clock Valid	tKHCOV	--	0.45	--	0.45	--	0.45	--	0.45	--	0.5	
C, \overline{C} Clock High to Echo Clock Valid	tCHCOV											
K, \overline{K} Clock High to Echo Clock Hold	tKHCOX	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.5	--	
C, \overline{C} Clock High to Echo Clock Hold	tCHCOX											
CQ, \overline{CQ} High Output Valid	tCQHQV	--	0.25	--	0.27	--	0.30	--	0.35	--	0.40	7
CQ, \overline{CQ} High Output Hold	tCQHQX	0.25	--	0.27	--	0.30	--	0.35	--	0.40	--	7
K Clock High to Data Output High-Z	tKHQZ	--	0.45	--	0.45	--	0.45	--	0.45	--	0.5	3
C Clock High to Data Output High-Z	tCHQZ											
K Clock High to Data Output Low-Z	tKHQX1	-0.45	--	-0.45	--	-0.45	--	-0.45	--	-0.5	--	3
C Clock High to Data Output Low-Z	tCHQX1											
Setup Times												
Address Input Setup Time	tAVKH	0.4	--	0.4	--	0.5	--	0.6	--	0.7	--	
Control Input Setup Time	tIVKH	0.4	--	0.4	--	0.5	--	0.6	--	0.7	--	2
Data Input Setup Time	tDVKH	0.28	--	0.3	--	0.35	--	0.4	--	0.5	--	
Hold Times												
Address Input Hold Time	tKHAX	0.4	--	0.4	--	0.5	--	0.6	--	0.7	--	
Control Input Hold Time	tKHIX	0.4	--	0.4	--	0.5	--	0.6	--	0.7	--	
Data Input Hold Time	tKHDX	0.28	--	0.3	--	0.35	--	0.4	--	0.5	--	

Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are R/ \overline{W} and $\overline{B}W_n$.
3. If C clocks are tied high, K clocks become the references for C clock timing parameters.

4. To avoid bus contention, at any given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9 V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7 V). It is not possible for two SRAMs on the same board to be at such different voltages and temperatures.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. DLL Lock Time (tKClock) is a minimum of 1024 cycles in all cases. Vdd slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. tKClock begins once Vdd and input clock are stable.
7. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guard bands and test setup variations.

Programmable Impedance HSTL Output Driver DC Electrical Characteristics (V)

Parameter	Symbol	Condition	Min	Max	Notes
Output High Voltage	VOH	RQ = 250• and VDDQ = 1.5 V or 1.8 V	VDDQ/2	VDDQ	1
		Minimum Impedance mode, ZQ = VSS	VDDQ - 0.2	VDDQ	2
Output Low Voltage	VOL	RQ = 250• and VDDQ = 1.5 V or 1.8 V	VSS	VDDQ/2	3
		Minimum Impedance mode, ZQ = VSS	VSS	0.2	4

Notes:

1. IOH = - (VDDQ/2) / (RQ/5) +/- 15% @ VOH = VDDQ/2 (for: 175Ω ≤ RQ ≤ 350Ω).
2. IOH = -1.0 mA
3. IOL = (VDDQ/2) / (RQ/5) +/- 15% @ VOL = VDDQ/2 (for: 175Ω ≤ RQ ≤ 350Ω).
4. IOL = 1.0 mA

Operating Currents

Parameter	Test Conditions	Symbol	-333		-300		-250		-200		-167	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
x36 Operating Current	VDD = max, IOUT = 0 mA Cycle time • tKHKH Min	IDD	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
x18 Operating Current		IDD	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
x9 Operating Current		IDD	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd
Standby Current (NOP)	Device deselected, IOUT = 0 mA, f = max, Inputs • 0.2 V or • VDD - 0.2V	ISB1	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd

Notes:

Power measured with output pins floating.

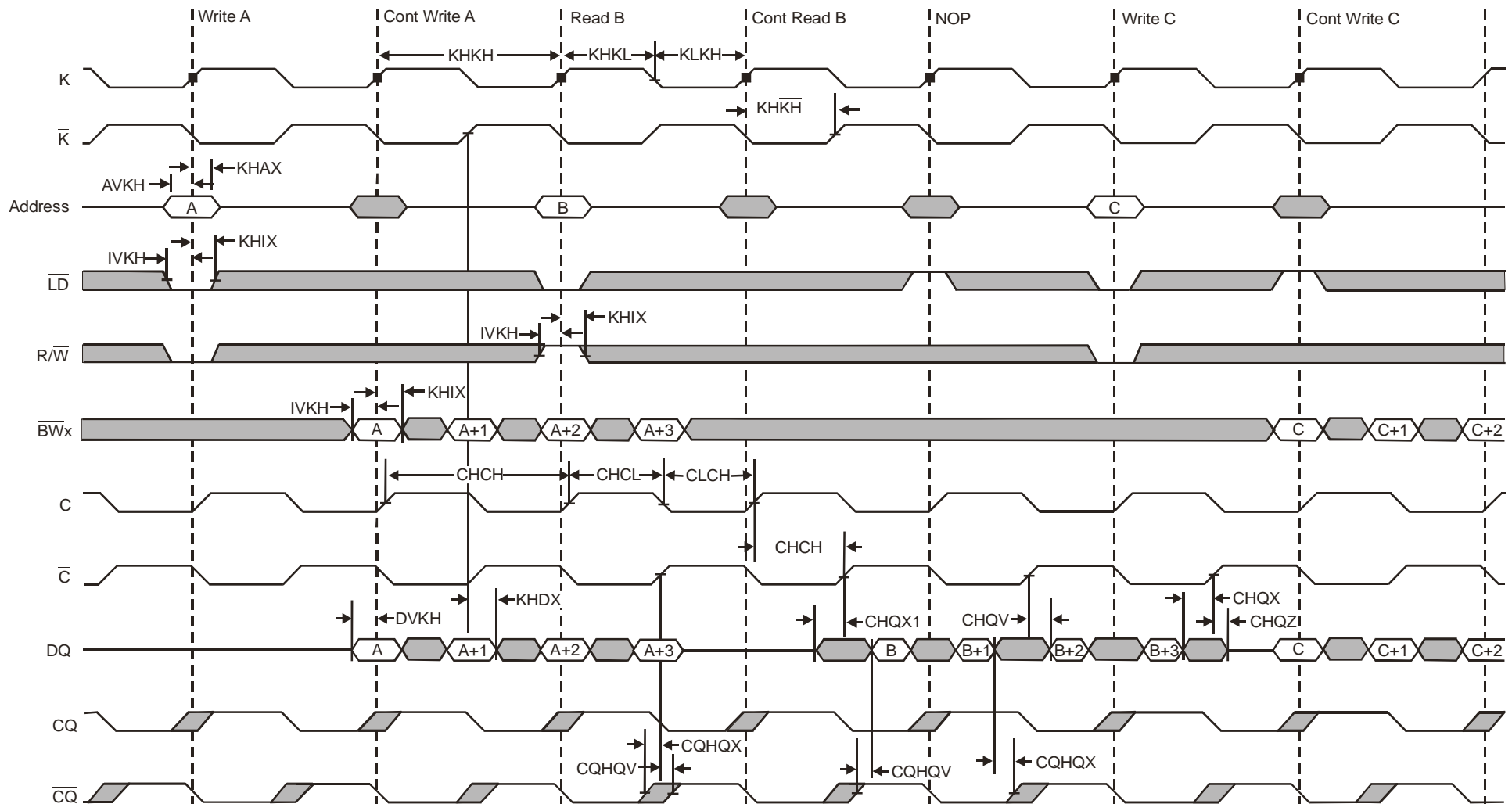
Minimum cycle, IOUT = 0 mA

Operating current is calculated with 50% read cycles and 50% write cycles.

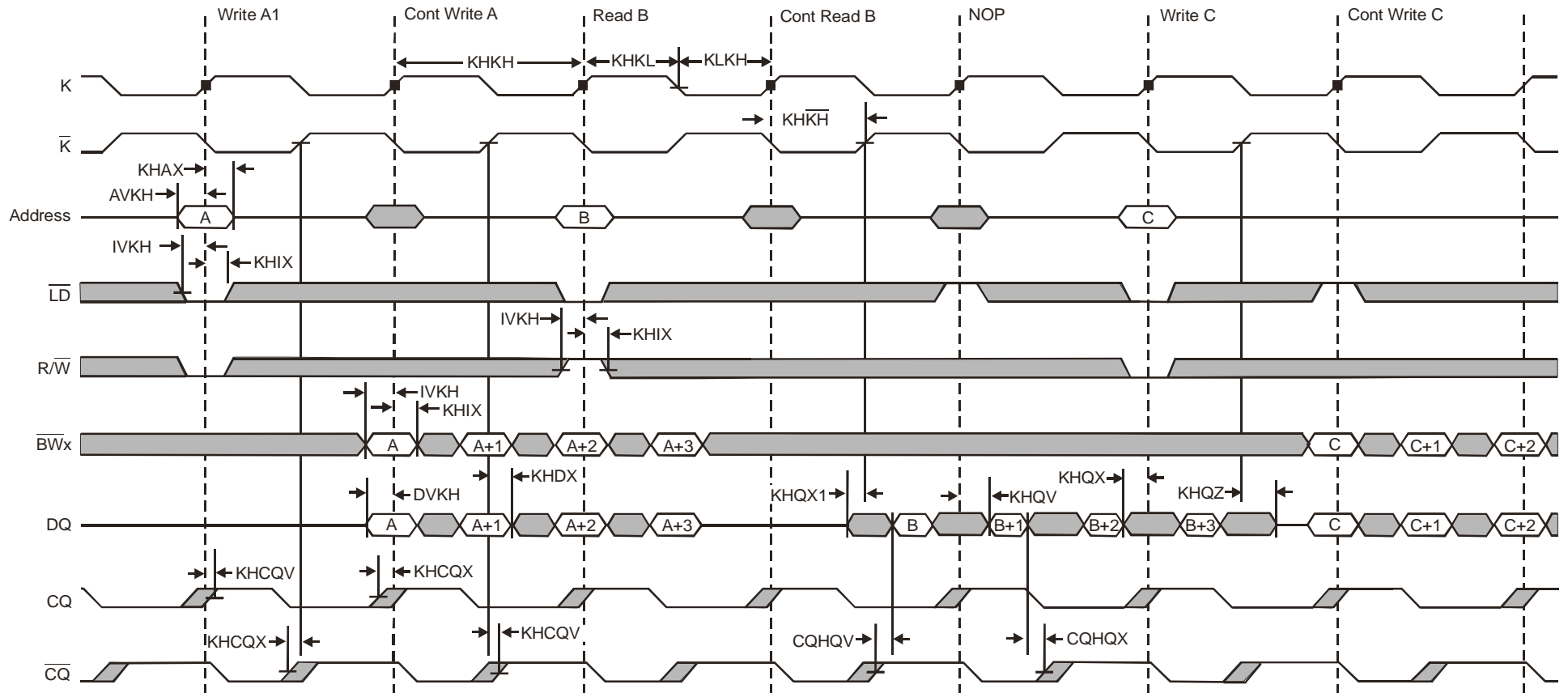
Standby Current is only after all pending read and write burst operations are completed.

Timing Diagrams

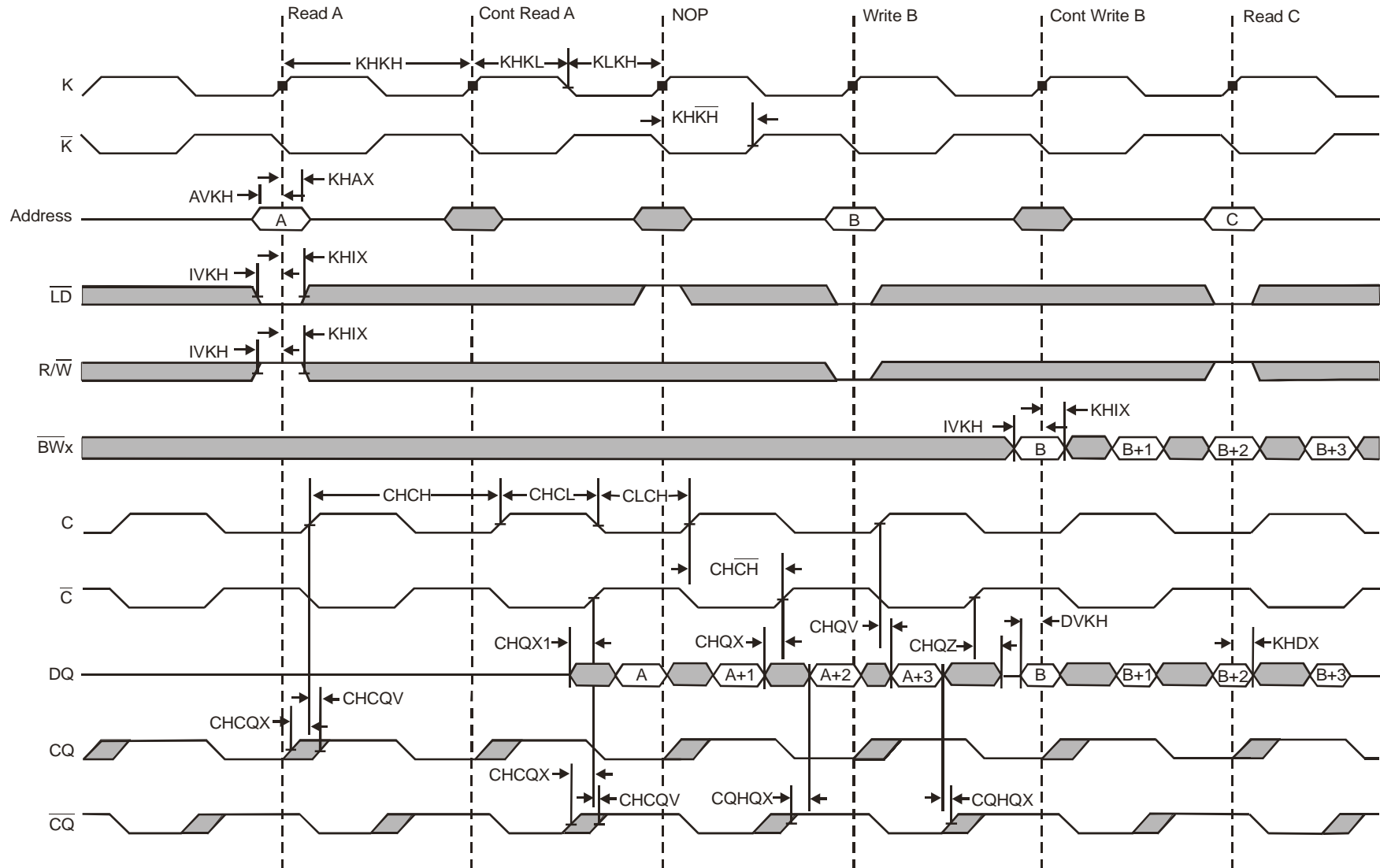
C and \bar{C} Controlled Write-Read-Write



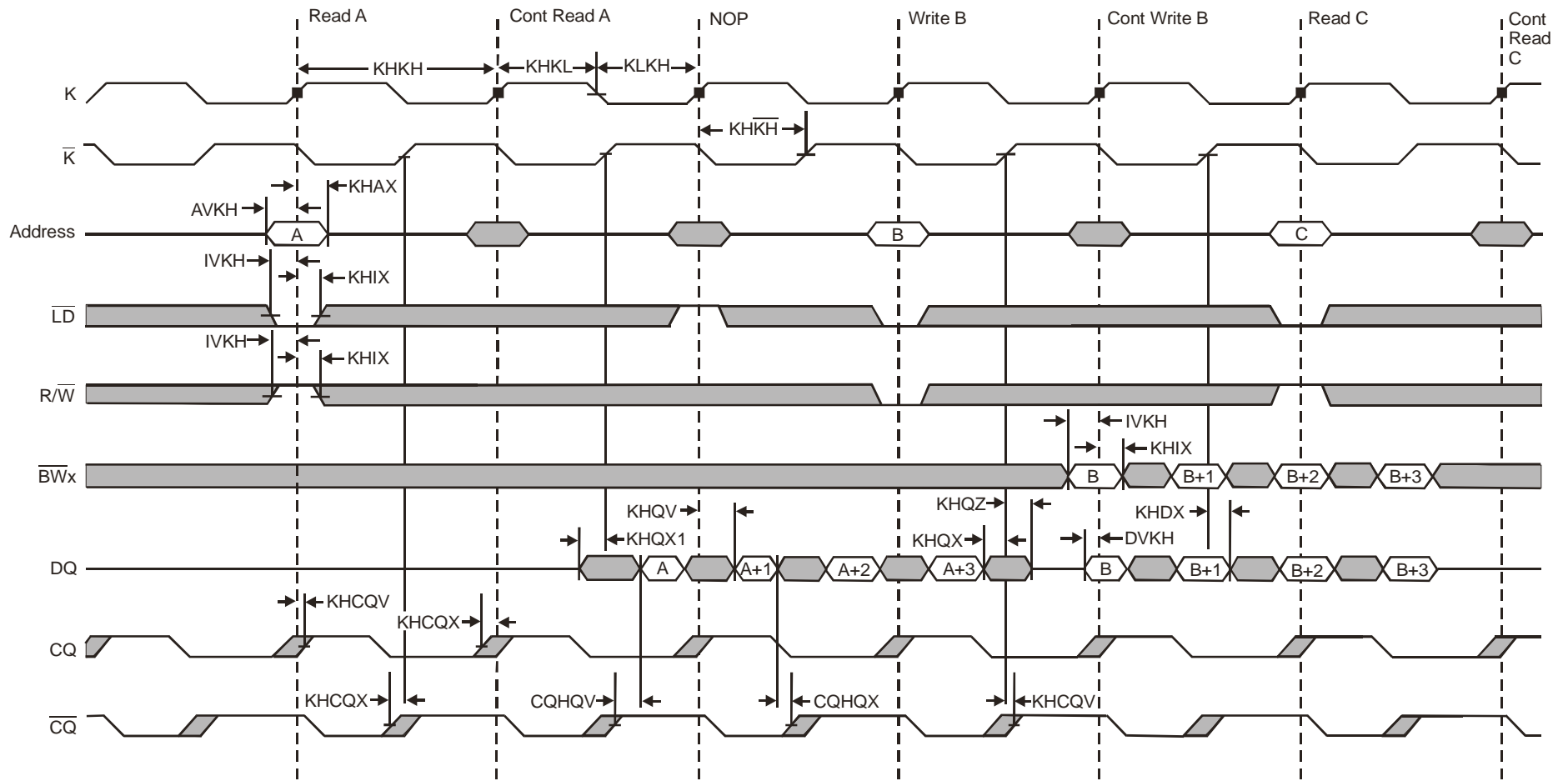
K and \bar{K} Controlled Write-Read-Write



C and \bar{C} Controlled Read-Write-Read



K and \bar{K} Controlled Read-Write-Read



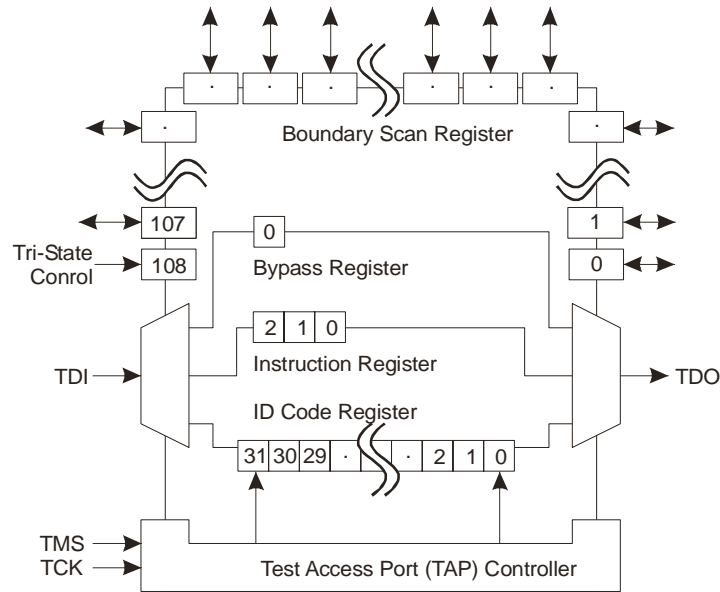
JTAG Port Operation

Overview

This device incorporates a serial boundary scan interface that complies with IEEE Standard 1149.1-1990, commonly known as JTAG. The JTAG Port is also known as a Test Access Port, or TAP. It can be used to read the device ID code, monitor all RAM input and I/O pads, drive pre-loaded values into the I/O bus, or the I/O bus to a High-Z state.

The port's input interface levels scale with VDD and the output drivers are powered by VDDQ. The port is reset at power-up and remains inactive until clocked. Pins, registers, states, and instructions are described below.

JTAG Test Access Port Block Diagram



JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all events. Inputs are captured on the rising edge; outputs are driven on the falling edge.
TMS	Test Mode Select	In	Command input for the JTAG state machine, sampled on the rising edge of TCK.
TDI	Test Data In	In	The input side of any selected register, sampled on the rising edge of TCK.
TDO	Test Data Out	Out	The output side of any selected register, driven on the falling edge of TCK.

Notes: TCK, TDI, and TMS have internal pull-up circuits; when undriven they produce a logic one input level.

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The JTAG controller is reset automatically at power-up, and again whenever it enters the Test-Logic-Reset state.

The "selected" register is determined by the current instruction and the state of the JTAG controller.

Disabling the JTAG Port

For normal operation of the device without using JTAG, the controller can be held in a permanent Reset state. To do this, TCK, TDI, and TMS are left floating or tied to either VDD or VSS. TDO should be left unconnected.

JTAG Registers

The JTAG interface has four serial shift registers that are used in conjunction with JTAG instructions. When a register is selected, it is placed between TDI and TDO so that it can shift data out serially on the falling edges of TCK and capture input data on the rising edges of TCK, depending on the state of the controller.

Instruction Register

The three-bit Instruction Register holds an instruction to be executed. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller enters the Test-Logic-Reset state. The user may load instructions through the TDI pin using the various IR (Instruction Register) states. The Instruction Register is always selected in the IR states, regardless of the current instruction.

Bypass Register

The single-bit Bypass Register can be placed between TDI and TDO to pass serial data through the JTAG Port with as little delay as possible. The Bypass Register is selected by the BYPASS instruction.

Identification (ID) Register

The 32-bit ID Register receives an identification code from an on-chip ID ROM. The code describes various attributes of the RAM as indicated in the table below. The ID Register is selected by the IDCODE instruction.

ID Code Contents

Bit#	Die Revision Code				Not Used								I/O Configuration								Tezzaron Semiconductor JEDEC Vendor ID Code								Presence Register				
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4		3	2	1	0
x36	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1
x16	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0	0	1
x9	X	X	X	X	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0	0	0	1	0	1	1	0	0	1

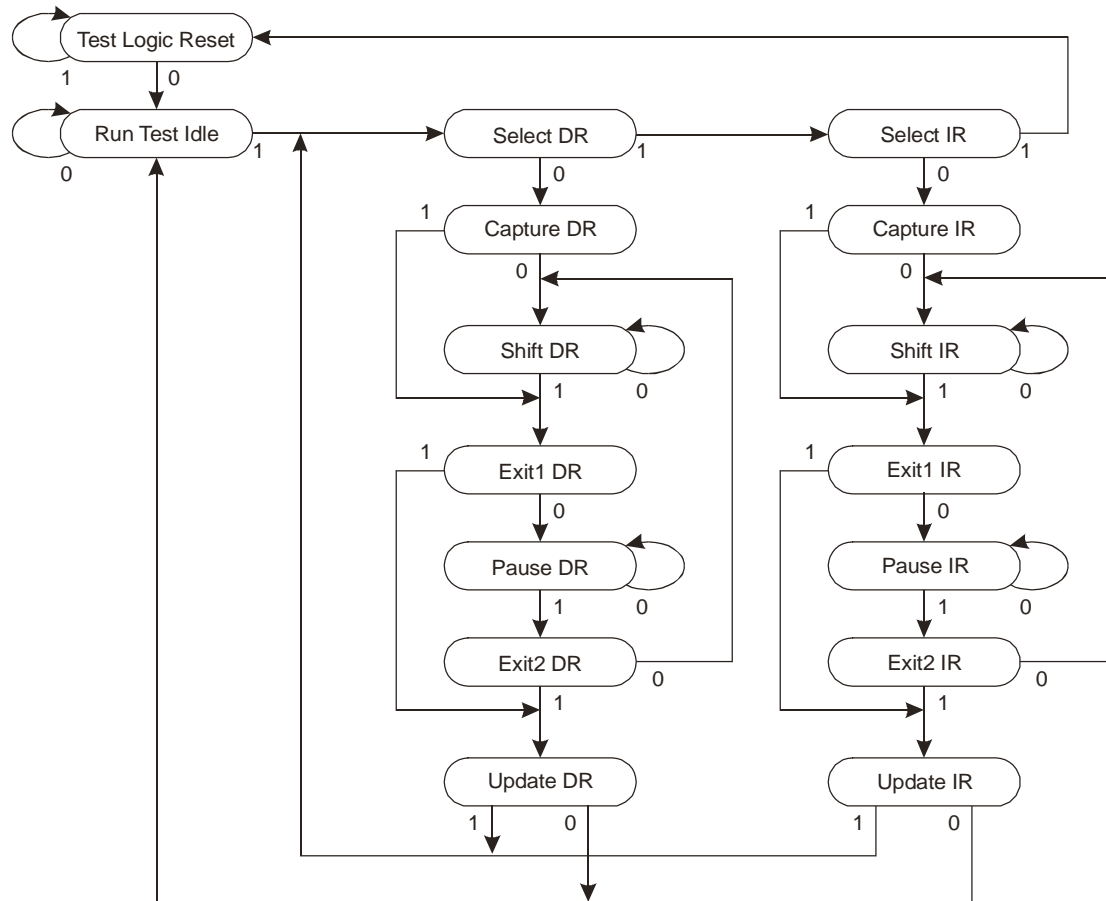
Boundary Scan Register

The Boundary Scan Register is a chain of 109 cells. Each cell contains a Scan bit and an Update bit. The Scan bits can capture the logic level found on the RAM's I/O pins; the Update bits can drive a preloaded set of data onto the RAM's outputs. The Boundary Scan Register cells are daisy chained together so their contents can be shifted out serially through the TDO pin and loaded through the TDI pin. The relationship between the device pins and the cells in the Boundary Scan Register is described in the Scan Order Table below; note that the register includes a number of special purpose cells that do not represent I/O pins. The Boundary Scan Register is selected by the SAMPLE-Z, SAMPLE/PRELOAD, and EXTEST instructions.

Scan Order Table

Cell#	Pin Name	I/O	Notes	Cell#	Pin Name	I/O	Notes	Cell#	Pin Name	I/O	Notes	Cell#	Pin Name	I/O	Notes
0	tbd	tbd		28	tbd	tbd		56	tbd	tbd		84	tbd	tbd	
1	tbd	tbd		29	tbd	tbd		57	tbd	tbd		85	tbd	tbd	
2	tbd	tbd		30	tbd	tbd		58	tbd	tbd		86	tbd	tbd	
3	tdb	tbd		31	tdb	tbd		59	tdb	tbd		87	tdb	tbd	
4	tbd	tbd		32	tbd	tbd		60	tbd	tbd		88	tbd	tbd	
5	tbd	tbd		33	tbd	tbd		61	tbd	tbd		89	tbd	tbd	
6	tbd	tbd		34	tbd	tbd		62	tbd	tbd		90	tbd	tbd	
7	tdb	tbd		35	tdb	tbd		63	tdb	tbd		91	tdb	tbd	
8	tdb	tdb		36	tdb	tdb		64	tdb	tdb		92	tdb	tdb	
9	tdb	tdb		37	tdb	tdb		65	tdb	tdb		93	tdb	tdb	
10	tdb	tdb		38	tdb	tdb		66	tdb	tdb		94	tdb	tdb	
11	tdb	tdb		39	tdb	tdb		67	tdb	tdb		95	tdb	tdb	
12	tdb	tdb		40	tdb	tdb		68	tdb	tdb		96	tdb	tdb	
13	tdb	tdb		41	tdb	tdb		69	tdb	tdb		97	tdb	tdb	
14	tdb	tdb		42	tdb	tdb		70	tdb	tdb		98	tdb	tdb	
15	tdb	tdb		43	tdb	tdb		71	tdb	tdb		99	tdb	tdb	
16	tdb	tdb		44	tdb	tdb		72	tdb	tdb		100	tdb	tdb	
17	tdb	tdb		45	tdb	tdb		73	tdb	tdb		101	tdb	tdb	
18	tdb	tdb		46	tdb	tdb		74	tdb	tdb		102	tdb	tdb	
19	tdb	tdb		47	tdb	tdb		75	tdb	tdb		103	tdb	tdb	
20	tdb	tdb		48	tdb	tdb		76	tdb	tdb		104	tdb	tdb	
21	tdb	tdb		49	tdb	tdb		77	tdb	tdb		105	tdb	tdb	
22	tdb	tdb		50	tdb	tdb		78	tdb	tdb		106	tdb	tdb	
23	tdb	tdb		51	tdb	tdb		79	tdb	tdb		107	tdb	tdb	
24	tdb	tdb		52	tdb	tdb		80	tdb	tdb		108	Tri-State Control	n/a	
25	tdb	tdb		53	tdb	tdb		81	tdb	tdb					
26	tdb	tdb		54	tdb	tdb		82	tdb	tdb					
27	tdb	tdb		55	tdb	tdb		83	tdb	tdb					

JTAG Controller State Diagram



JTAG Controller States

Overview

The JTAG controller is inactive until clocked with TCK. When TCK is activated, the controller is in the Test Logic Reset state. Subsequent transitions between states are controlled by the TMS signal as shown in the diagram above. TMS is sampled at each rising edge of TCK.

The DR states select and manipulate the four JTAG data registers; the IR states select and manipulate the Instruction Register.

Test Logic Reset

In this state, the IDCODE instruction is loaded into the Instruction Register, no control is exerted over the RAM's output pins, and the RAM executes as if the JTAG port were disabled. If TMS is held at 1 for five cycles, the controller returns to this state and loops until it detects a TMS value of 0.

Run Test Idle

This is the entry point for all instructions. The controller can loop here as needed, but performs no functions.

Select DR

The controller selects a data register (determined by the current instruction) and places it between TDI and TDO.

Capture DR

Depending upon the current instruction, the selected register may receive data from sources other than TDI.

Shift DR

On the falling edge of TCK, the least significant bit of the selected register is shifted onto TDO. On the rising edge of TCK, the value on the TDI pin is captured and shifted into the most significant bit of the selected register.

Exit1 DR

Data movement stops. No function is performed.

Pause DR

The controller can loop here, but performs no functions.

Exit2 DR

No function is performed.

Update DR

If the current instruction is SAMPLE or EXTEST, data in the Boundary Scan Register is copied from the Scan bits to the Update bits. Otherwise, no function is performed.

Select IR

The Instruction Register is selected and placed between TDI and TDO.

Capture IR

The controller loads the two least significant bits of the Instruction Register with 01.

Shift IR, Exit1 IR, Pause IR, Exit2 IR

These states are analogous to Shift DR, Exit1 DR, Pause DR, and Exit2 DR.

Update IR

Instruction loading is complete; the instruction is decoded for implementation. If the new instruction is EXTEST or SAMPLE-Z, JTAG exerts control over the RAM's output pins; otherwise, it releases control of those pins.

JTAG Controller Instruction Set

Instruction Summary

Instruction	Binary Code	Description
EXTEST	000	Either drives contents onto RAM outputs or forces outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
IDCODE	001	Selects and loads ID Register; allows reading of register. Default instruction – automatically loaded in test-logic-reset state.
SAMPLE-Z	010	Forces all RAM outputs to High-Z; selects Boundary Scan Register; captures I/O ring contents; allows reading of Boundary Scan Register.
RFU	011	Do not use this instruction; reserved for future use. (Currently replicates BYPASS instruction.)
SAMPLE/PRELOAD	100	Selects Boundary Scan Register; captures I/O ring contents; allows reading/loading of Boundary Scan Register.
TEZZARON	101	Tezzaron private instruction; do not use.
RFU	110	Do not use this instruction; Reserved for Future Use. (Currently replicates BYPASS instruction.)
BYPASS	111	Selects Bypass Register; allows rapid pass-through of data.

Instruction Descriptions

NOTE: Several of these instructions capture signals from the RAM's I/O ring. The user must be aware that the JTAG clock (TCK) operates at 20 MHz or less, while the RAM clock operates more than an order of magnitude faster. Because of the difference in clock frequencies, it is possible that an input or output will undergo a transition during the capture. In this case, the signal may be captured while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured, and repeatable results may not be possible. To guarantee that the correct value of a signal is captured, the signal must be stabilized long enough to meet the JTAG set-up plus hold times ($t_{TS} + t_{TH}$). If there is no way in a design to stop (or slow) the RAM clock, the RAM clock inputs might not be captured correctly; however, it is still possible to capture all other signals and simply ignore the captured values of the RAM clock signals.

BYPASS

This instruction allows test data to pass through the device with minimal delay, to facilitate testing of other devices on the scan path.

Select-DR: The Bypass Register is placed between TDI and TDO.

Shift-DR: Data is shifted out through TDO and in from TDI.

SAMPLE/PRELOAD

This instruction allows sample data to be captured and examined without interfering with normal device operation. It also allows test data to be pre-loaded for later use with the EXTEST instruction.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data from the Scan bits is copied into the Update bits for later use (see EXTEST).

EXTEST

This instruction captures sample data and sets up test data, much like SAMPLE/PRELOAD, but it also controls the RAM's output pins. EXTEST is for testing only, as it will disrupt normal operation of the device. As soon as the EXTEST instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded. The values in the Boundary Scan Register's Update bits are driven onto the output pins, *unless the Tri-State Control cell has been set (see below)*, in which case the output pins are tri-stated.

EXTEST and Tri-State

The Boundary Scan Register's last cell, #108, is the Tri-State Control cell. During EXTEST, it directly controls the state of the RAM's output pins. When HIGH, it enables the Update bit values to drive the output bus; when LOW, it places the output bus into a High-Z condition. The Tri-State Control cell's value is set to HIGH whenever the controller is in the "Test-Logic-Reset" state. The value is changed with the SAMPLE/PRELOAD or EXTEST instruction by shifting the desired value into the cell during the Shift-DR state. During Update-DR, the new value is copied into the cell's Update bit. From there, it controls the EXTEST instruction's behavior.

Select-DR: The Boundary Scan Register is placed between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits of the cells.

Shift-DR: Data in the Scan bits is shifted out serially through TDO and data presented to TDI is shifted in.

Update-DR: Data in the Scan bits is copied to the Update bits. The values take effect immediately, driving the RAM's output bus as directed.

IDCODE

IDCODE is the default instruction, loaded automatically whenever the controller is placed in the Test-Logic-Reset state. It allows access to the device's internal ID ROM contents.

Select-DR: The ID Register is placed between TDI and TDO.

Capture-DR: The ID Register is loaded with the device's 32-bit identification code from the ID ROM.

Shift-DR: The contents of the ID Register is shifted out through TDO.

SAMPLE-Z

This instruction functions somewhat like EXTEST, except that the output bus is always tri-stated and the Update bits are not changed. Like EXTEST, it is disruptive to normal device operation. As soon as the SAMPLE-Z instruction is loaded (in Update-IR), it exerts control over the RAM's output pins and does not release them until a new instruction is loaded.

Select-DR: The Boundary Scan Register is connected between TDI and TDO.

Capture-DR: A snapshot of data from all the RAM's I/O pins is captured in the Scan bits.

Shift-DR: Data in the Scan bits is shifted out serially through TDO.

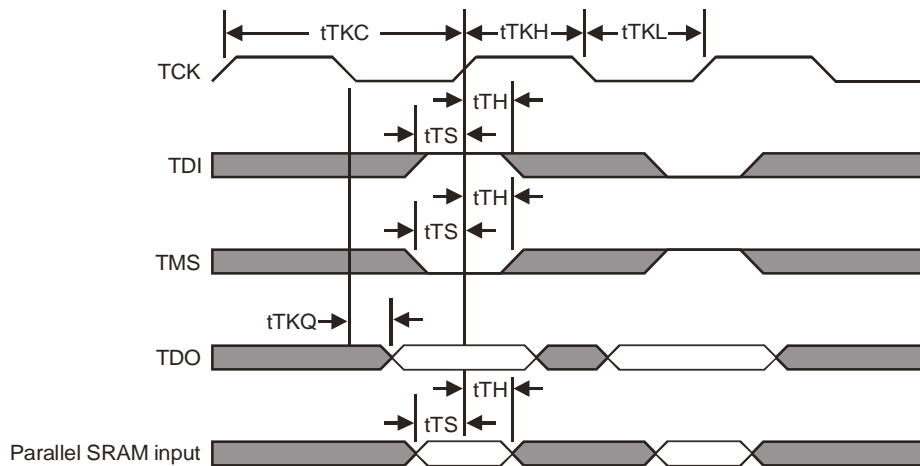
Tezzaron

This instruction is reserved for vendor use; do not use.

RFU

This instruction is reserved for future use; in this device it replicates the BYPASS instruction.

JTAG Port Timing Diagram



JTAG Port Recommended Operating Conditions and DC Characteristics (V)

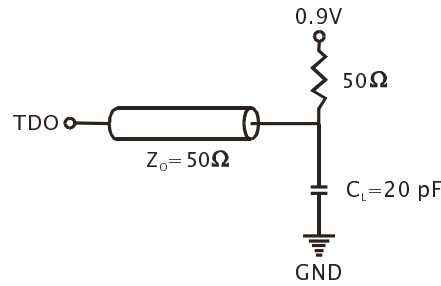
Parameter	Symbol	Min.	Typ.	Max.
Power Supply Voltage	VDDQ	1.7	1.8	1.9
Input High Voltage	V _{IH}	1.3	--	VDD + 0.3
Input Low Voltage	V _{IL}	-0.3	--	0.5
Output High Voltage (I _{OH} = -2 mA)	V _{OH}	1.4	--	VDD
Output Low Voltage (I _{OL} = 2 mA)	V _{OL}	V _{SS}	--	0.4

Note: During JTAG operation, the input level of the RAM pins must conform to the device's DC specifications.

JTAG Port AC Test Conditions

Parameter	Symbol	Min	Unit
Input High/Low Level	V _{IH} /V _{IL}	1.3/0.5	V
Input Rise/Fall Time	T _R /T _F	1.0/1.0	ns
Input and Output Timing Reference Level	--	0.9	V

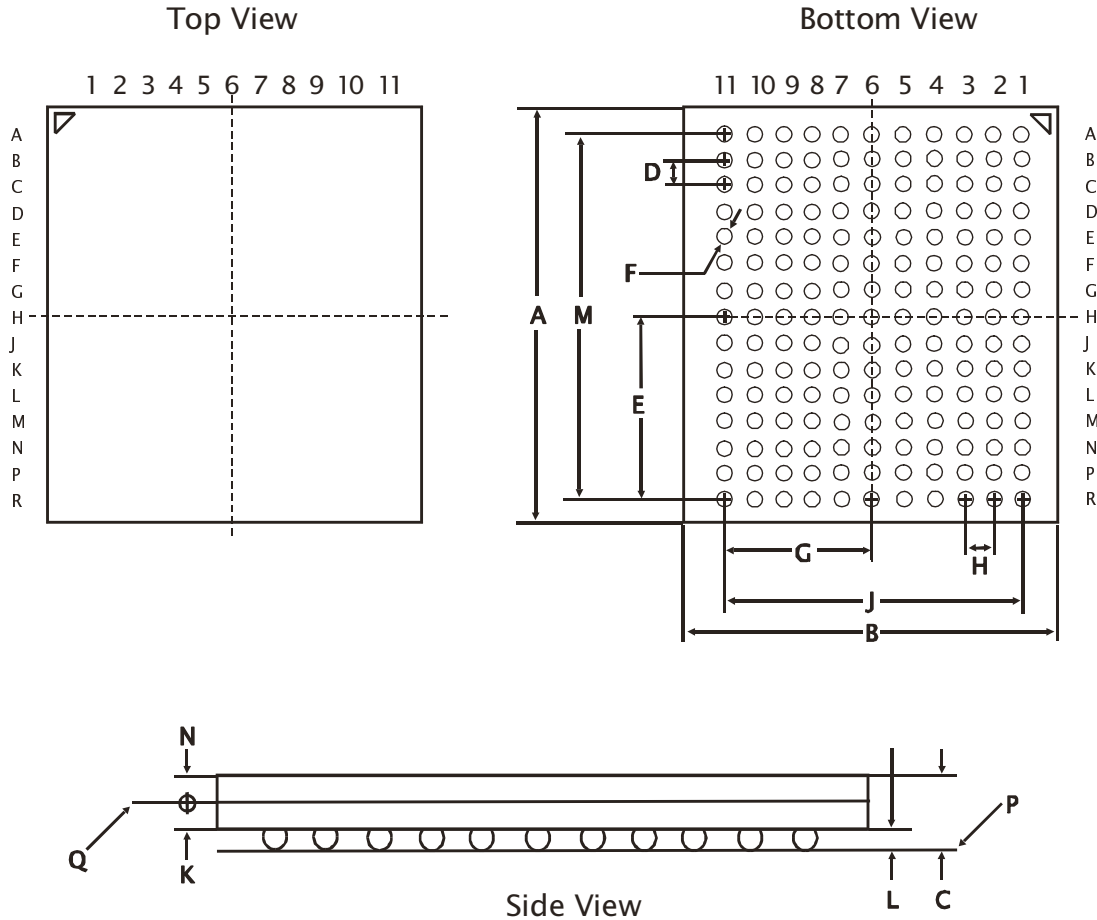
Parameters are measured with distributed scope and test jig capacitance.
Conditions as shown in diagram below unless otherwise noted.



JTAG Port AC Electrical Characteristics (ns)

Parameter	Symbol	Min	Max
TCK Cycle Time	tTKC	50	—
TCK High Pulse Width	tTKH	20	—
TCK Low Pulse Width	tTKL	20	—
Set Up Time – (TDI, TMS, Capture)	tTS	5	—
Hold Time – (TDI, TMS, Capture)	tTH	5	—
TCK Low to TDO Valid	tTKQ	0	10

Package Drawing



Symbol	Description	Measurement (mm)
A	Chip Length	17.00±0.10
B	Chip Width	15.00±0.10
C	Chip Height	1.40 max.
D	Length between pin centers	1.00
E	Length between center pin and outermost pin	7.00
F	Pin diameter	0.50 +0.14 / -0.06
G	Width between center pin and outermost pin	5.00
H	Width between pin centers	1.00
J	Width between outermost pins	10.00
K	Height of circuit card	0.36
L	Height of pins	0.35±0.06

Symbol	Description	Measurement (mm)
M	Length between outermost pins	14.00
N	Height of encapsulant	0.53±0.05
P	Seating Plane *	
Q	Top Plane of circuit card **	

Pin centers: within 0.05 mm of relative position at MMC
Pin centers: within 0.25 mm of true position at MMC
Package length/width edges: uniform within 0.15 mm
Package weight: tbd
Solder pad type NSMD (non-solder mask defined)
JEDEC reference: MO-216 – design 4.6C

* Seating plane surface uniform within 0.15 mm

** Top plane parallel to seating plane within 0.25 mm

Document History

Datasheet for TSC3D472C09 / 18 / 36

Revision	Date	Changes
1.0	September 13, 2006	Original
1.1	23 January 2007	Added package letter, added DTRII trademark, corrected typos

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